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* * * * * * * * * *   Welcome to STN International   * * * * * * * * * *

 NEWS  1           Web Page URLs for STN Seminar Schedule - N. America
 NEWS  2           "Ask CAS" for self-help around the clock
 NEWS  3  FEB 27   New STN AnaVist pricing effective March 1, 2006
 NEWS  4  MAY 10   CA/CAplus enhanced with 1900-1906 U.S. patent records
 NEWS  5  MAY 11   KOREAPAT updates resume
 NEWS  6  MAY 19   Derwent World Patents Index to be reloaded and enhanced
 NEWS  7  MAY 30   IPC 8 Rolled-up Core codes added to CA/CAplus and
                   USPATFULL/USPAT2
 NEWS  8  MAY 30   The F-Term thesaurus is now available in CA/CAplus
 NEWS  9  JUN 02   The first reclassification of IPC codes now complete in
                   INPADOC
 NEWS 10  JUN 26   TULSA/TULSA2 reloaded and enhanced with new search and
                   and display fields
 NEWS 11  JUN 28   Price changes in full-text patent databases EPFULL and PCTFULL
 NEWS 12  JUl 11   CHEMSAFE reloaded and enhanced
 NEWS 13  JUl 14   FSTA enhanced with Japanese patents
 NEWS 14  JUl 19   Coverage of Research Disclosure reinstated in DWPI
 NEWS 15  AUG 09   INSPEC enhanced with 1898-1968 archive
 NEWS 16  AUG 28   ADISCTI Reloaded and Enhanced
 NEWS 17  AUG 30   CA(SM)/CAplus(SM) Austrian patent law changes
 NEWS 18  SEP 11   CA/CAplus enhanced with more pre-1907 records
 NEWS 19  SEP 21   CA/CAplus fields enhanced with simultaneous left and right
                   truncation
 NEWS 20  SEP 25   CA(SM)/CAplus(SM) display of CA Lexicon enhanced
 NEWS 21  SEP 25   CAS REGISTRY(SM) no longer includes Concord 3D coordinates
 NEWS 22  SEP 25   CAS REGISTRY(SM) updated with amino acid codes for pyrrolysine
 NEWS 23  SEP 28   CEABA-VTB classification code fields reloaded with new
                   classification scheme

 NEWS EXPRESS  JUNE 30 CURRENT WINDOWS VERSION IS V8.01b, CURRENT
               MACINTOSH VERSION IS V6.0c(ENG) AND V6.0Jc(JP),
               AND CURRENT DISCOVER FILE IS DATED 26 JUNE 2006.

 NEWS HOURS    STN Operating Hours Plus Help Desk Availability
 NEWS LOGIN    Welcome Banner and News Items
 NEWS IPC8     For general information regarding STN implementation of IPC 8
 NEWS X25      X.25 communication option no longer available

Enter NEWS followed by the item number or name to see news on that
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FILE 'HOME' ENTERED AT 17:52:04 ON 17 OCT 2006

=> file inspec
FILE 'INSPEC' ENTERED AT 17:52:29 ON 17 OCT 2006
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FILE LAST UPDATED: 16 OCT 2006       <20061016/UP>
FILE COVERS 1898 TO DATE.

<<< SIMULTANEOUS LEFT AND RIGHT TRUNCATION AVAILABLE IN
    THE ABSTRACT (/AB), BASIC INDEX (/BI) AND TITLE (/TI) FIELDS  >>>

<<< INSPEC HAS BEEN ENHANCED WITH ARCHIVE DATA 1898-1968
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    --> SEE NEWS
        AND HELP CHANGE (last updated Aug 11, 2006)  >>>

=> e muraka/au
E1            2     MURAJI T/AU
E2            4     MURAJI Y/AU
E3            0 --> MURAKA/AU
E4            1     MURAKA S/AU
E5            5     MURAKA S P/AU
E6            1     MURAKADO C/AU
E7            1     MURAKADO S/AU
E8            1     MURAKAM H/AU
E9            1     MURAKAM K/AU
E10           1     MURAKAM M/AU
E11           2     MURAKAM S/AU
E12           1     MURAKAMA T/AU

=> e5
L1            5 "MURAKA S P"/AU

=> d 1-5 ti

L1   ANSWER 1 OF 5  INSPEC  (C) 2006 IET on STN
 Citing
References
TI    Low-temperature passivation of copper by doping with Al or Mg

L1   ANSWER 2 OF 5  INSPEC  (C) 2006 IET on STN
 Citing
References
TI    Thermal stability of on-chip copper interconnect structures

L1   ANSWER 3 OF 5  INSPEC  (C) 2006 IET on STN
 Citing
References
TI    The coupling of an N-well CMOS fabrication laboratory course with the
      SEMATECH Center of Excellence in Multilevel Metallization at Rensselaer

L1   ANSWER 4 OF 5  INSPEC  (C) 2006 IET on STN
 Citing
References
TI    Recent advances in silicide technology

L1   ANSWER 5 OF 5  INSPEC  (C) 2006 IET on STN
 Citing
References
TI    A study of stacking faults during CMOS processing: origin, elimination
      and contribution to leakage


=> d 4 ab

L1   ANSWER 4 OF 5  INSPEC  (C) 2006 IET on STN
 Citing
References
AB    Recent advances in silicide technology are reviewed. Single target
      sputtering, CVD techniques, awareness of properly carried out oxidation,
      use of self-aligned silicides and rapid thermal annealing, and new
      applications are discussed


=> d 4 all

L1   ANSWER 4 OF 5  INSPEC  (C) 2006 IET on STN
 Full  Citing
 Text  References
AN    1986:2594256  INSPEC     DN  B1986-009061
TI    Recent advances in silicide technology
```

AU **Muraka, S.P.** (Center for Integrated Electron., Rensselaer Polytech. Inst., Troy, NY, USA)
SO Solid State Technology (Sept. 1985), vol.28, no.9, p. 181-5, 32 refs.
CODEN: SSTEAP, ISSN: 0038-111X
DT Journal
TC Practical
CY United States
LA English
AB Recent advances in silicide technology are reviewed. Single target sputtering, CVD techniques, awareness of properly carried out oxidation, use of self-aligned silicides and rapid thermal annealing, and new applications are discussed
CC B0520F Chemical vapour deposition; B2550F Metallisation and interconnection technology
CT annealing; CVD coatings; integrated circuit technology; metallisation; sputtered coatings
ST silicide technology; sputtering; CVD techniques; oxidation; self-aligned silicides; rapid thermal annealing

=> (refractory and silicides and circuits)/ti
2759 REFRACTORY/TI
1409 SILICIDES/TI
49404 CIRCUITS/TI
L2 2 (REFRACTORY AND SILICIDES AND CIRCUITS)/TI

=> d 1,2 ti

L2 ANSWER 1 OF 2 INSPEC (C) 2006 IET on STN
Citing References
TI **Refractory** metal **silicides** for self-aligned gate modulation doped n+-(Al,Ga)As/GaAs field-effect transistor integrated **circuits**

L2 ANSWER 2 OF 2 INSPEC (C) 2006 IET on STN
Citing References
TI **Refractory silicides** for integrated **circuits**

=> d 2 all

L2 ANSWER 2 OF 2 INSPEC (C) 2006 IET on STN
Full Text Citing References
AN 1980:1596589 INSPEC DN A1980-100820; B1980-053689
TI **Refractory silicides** for integrated **circuits**
AU Murarka, S.P. (Bell Labs., Murray Hill, NJ, USA)
SO Journal of Vacuum Science and Technology (July-Aug. 1980), vol.17, no.4, p. 775-92, 77 refs.
CODEN: JVSTAL, ISSN: 0022-5355
DT Journal
TC General Review
CY United States
LA English
AB Transition metal silicides have, in the past, attracted attention because of their usefulness as high temperature materials and in integrated circuits as Schottky barrier and ohmic contacts. More recently, with the increasing silicon integrated circuits (SIC) packing density, the line widths get narrower and the sheet resistance contribution to the RC delay increases. The possibility of using low resistivity silicides, which can be formed directly on the polysilicon, makes these silicides highly attractive. The usefulness of a silicide metallization scheme for integrated circuits depends, not only on the desired low resistivity, but also on the ease with which the silicide can be formed and patterned and on the stability of the silicides throughout device processing and during actual device usage. Various properties and the formation techniques of the silicides have been reviewed. Correlations between the various

properties and the metal or silicide electronic or crystallographic structure have been made to predict the more useful silicides for SIC applications. Special reference to the silicide resistivity, stress, and oxidizability during the formation and subsequent processing has been given. Various formation and etching techniques are discussed

CC A0130R Reviews and tutorial papers; resource letters; A6570 Thermal expansion and thermomechanical effects; A7330 Surface double layers, Schottky barriers, and work functions; A8120L Preparation of ceramics and refractories; A8160B Surface treatment and degradation of metals and alloys; A8160D Surface treatment and degradation of ceramics and refractories; B2530D Semiconductor-metal interfaces; B2550F Metallisation and interconnection technology

CT etching; integrated circuit technology; metallisation; ohmic contacts; oxidation; refractories; reviews; Schottky effect; thermal expansion; transition metal compounds

ST integrated circuits; Schottky barrier; ohmic contacts; packing density; line widths; sheet resistance; silicide metallization scheme; low resistivity; crystallographic structure; stress; etching techniques; transition metal silicides; refractory silicides; electronic structure; thermal expansion

```
=> (titanium and disilicide and technology)/ti
         18067 TITANIUM/TI
           568 DISILICIDE/TI
         78494 TECHNOLOGY/TI
L3           2 (TITANIUM AND DISILICIDE AND TECHNOLOGY)/TI

=> d 1,2 ti

L3   ANSWER 1 OF 2  INSPEC  (C) 2006 IET on STN
Citing References
TI    Titanium disilicide self-aligned source/drain+gate technology

L3   ANSWER 2 OF 2  INSPEC  (C) 2006 IET on STN
Citing References
TI    Titanium disilicide in MOS technology


=> d 1 all

L3   ANSWER 1 OF 2  INSPEC  (C) 2006 IET on STN
Full Text  Citing References
AN    1983:2048908  INSPEC     DN  B1983-030014
TI    Titanium disilicide self-aligned source/drain+gate technology
AU    Lau, C.K.; See, Y.C.; Scott, D.B.; Bridges, J.M.; Perna, S.M.; Davies,
      R.D. (CMOS Div., Texas Instruments Inc., Dallas, TX, USA)
SO    International Electron Devices Meeting. Technical Digest, 1982, p. 714-17
      of 812 pp., 10 refs.
      Price: CH1832-5/82/0000-0714$00.75
      Published by: IEEE, New York, NY, USA
      Conference: International Electron Devices Meeting. Technical Digest, San
      Francisco, CA, USA, 13-15 Dec. 1982
      Sponsor(s): IEEE
DT    Conference; Conference Article
TC    New Development; Practical
CY    United States
LA    English
AB    Silicides have been used to lower the resistance of gate level
      interconnects. Recently silicidation of source/drain diffusions have also
      been reported. In scaled CMOS devices, silicidation of source/drains is
      particularly important in reducing the sheet resistance of
      p+-source/drain diffusions. In this paper, a novel technique is described
      in which TiSi2 is formed self-aligned to both source/drain and gate
      regions. Both n- and p-channel MOSFETs silicided with self-aligned TiSi2
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on source/drains and gates have been fabricated using this technique. Sheet resistances below 5 Ω/.box. on both gate and source/drain levels have been achieved and thus represent at least a 10× reduction in the resistance of p+-diffusions. Diode leakage, subthreshold leakage, and threshold voltage measurements on silicided devices are comparable with that of control devices without silicidation. CMOS circuit applications of this TiSi2 self-aligned source-drain and gate technology are discussed
CC B2550F Metallisation and interconnection technology; B2570D CMOS integrated circuits
CT field effect integrated circuits; integrated circuit technology; large scale integration; metallisation; titanium compounds
ST TiSi2; IC technology; gate level interconnects; sheet resistance; MOSFETs; self-aligned TiSi2; source/drains; gates; CMOS circuit applications
ET Si; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi2; Ti cp; cp; Si cp

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* * * * * * RECONNECTED TO STN INTERNATIONAL * * * * * *
SESSION RESUMED IN FILE 'INSPEC' AT 18:02:30 ON 17 OCT 2006
FILE 'INSPEC' ENTERED AT 18:02:30 ON 17 OCT 2006

=> (titanium and halogen and lamp)/ti
18067 TITANIUM/TI
2261 HALOGEN/TI
4269 LAMP/TI
L4 3 (TITANIUM AND HALOGEN AND LAMP)/TI

=> d 1-3 ti

L4 ANSWER 1 OF 3 INSPEC (C) 2006 IET on STN
Citing References
TI Effects and behavior of arsenic during **titanium** silicidation by **halogen lamp** annealing

L4 ANSWER 2 OF 3 INSPEC (C) 2006 IET on STN
Citing References
TI **Titanium** silicidation by **halogen lamp** annealing

L4 ANSWER 3 OF 3 INSPEC (C) 2006 IET on STN
Citing References
TI **Titanium** silicidation by **halogen lamp** annealing

=> d 2,3 all

L4 ANSWER 2 OF 3 INSPEC (C) 2006 IET on STN
Full Text | Citing References
AN 1986:2636901 INSPEC DN A1986-045039; B1986-021346
TI **Titanium** silicidation by **halogen lamp** annealing
AU Okamoto, T.; Shimizu, M.; Tsukamoto, K.; Matsukawa, T. (LSI R&D Lab., Mitsubishi Electr. Corp., Hyogo, Japan)
SO Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, 1985, p. 471-6 of xix+740 pp., 7 refs.
Editor(s): Biegelsen, D.K.; Rozgonyi, G.A.; Shank, C.V.
ISBN: 0 931837 00 6
Published by: Mater. Res. Soc, Pittsburgh, PA, USA
Conference: Energy Beam-Solid Interactions and Transient Thermal Processing/1984 Symposium, Boston, MA, USA, 26-30 Nov. 1984
Sponsor(s): Mater. Res. Soc
DT Conference; Conference Article
TC Experimental
CY United States

LA English
AB Silicidation of titanium on silicon is carried out with halogen lamp annealing. The lamp annealing is quite effective in forming an oxide-free and homogeneous titanium disilicide layer with resistivity of 15-17 μohm·cm. Rutherford backscattering and X-ray diffraction studies show that halogen lamp annealing over 650°C for only 60 seconds results in disilicide formation. By a silicidation reaction, arsenic and boron atoms in silicon beneath a titanium layer are incorporated into a formed silicide layer. Arsenic atoms initially in a titanium layer are swept toward the surface as the silicidation reaction proceeds. Arsenic atoms in titanium have an effect of retarding the silicidation reaction
CC A6180 Radiation damage and other irradiation effects; A6180 Radiation damage and other irradiation effects; B2550 Semiconductor device technology
CT electrical conductivity of solids; impurities; incoherent light annealing; particle backscattering; titanium compounds; X-ray diffraction examination of materials
ST Ti silicidation; TiSi2; impurities; Si:As, B; incoherent light annealing; halogen lamp annealing; resistivity; Rutherford backscattering; X-ray diffraction; silicidation reaction
ET Si; As; C

L4 ANSWER 3 OF 3 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 1985:2514279 INSPEC DN A1985-101677; B1985-050272
TI **Titanium** silicidation by **halogen lamp** annealing
AU Okamoto, T.; Tsukamoto, K.; Shimizu, M.; Matsukawa, T. (LSI Res. & Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan)
SO Journal of Applied Physics (15 June 1985), vol.57, no.12, p. 5251-5, 15 refs.
CODEN: JAPIAU, ISSN: 0021-8979
Price: 0021-8979/85/125251-05$02.40
DT Journal
TC Experimental
CY United States
LA English
AB Silicidation of titanium (Ti) thin films sputter-deposited onto silicon (Si) was performed by the halogen lamp annealing method. This method was found to be quite effective in forming oxide-free and homogeneous titanium disilicide (TiSi2). Temperature dependence of silicidation was investigated by using Rutherford backscattering spectroscopy, X-ray diffraction, and sheet resistance measurements. It was found that the dominant crystal phase of silicide formed during annealing at 600 and 625°C for 90 sec was titanium monosilicide (TiSi), and that a homogeneous TiSi2 with resistivity of 15 μΩ cm was formed at 700°C. Self-aligned TiSi2 with low resistivity can be obtained with two-step annealing: the first-step annealing was carried out below 600°C and followed by removal of unreacted Ti on silicon dioxide (SiO2), and the second-step annealing was carried out above 650°C
CC A6180 Radiation damage and other irradiation effects; A6180 Radiation damage and other irradiation effects; A6630N Chemical interdiffusion in solids; A6848 Solid-solid interfaces; A7360D Electrical properties of metals and metallic alloys (thin films/low-dimensional structures); A7920N Atom-, molecule-, and ion-surface impact and interactions; B2530D Semiconductor-metal interfaces; B2550F Metallisation and interconnection technology
CT diffusion in solids; electronic conduction in metallic thin films; incoherent light annealing; interface structure; metallic thin films; metallisation; particle backscattering; semiconductor-metal boundaries; sputtered coatings; titanium; titanium compounds; X-ray diffraction examination of materials
ST TiSi; Ti silicidation; Ti sputter deposited thin films; temperature dependence; halogen lamp annealing; Rutherford backscattering spectroscopy; X-ray diffraction; sheet resistance measurements; dominant crystal phase; TiSi2; two-step annealing

ET Si; Ti; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi2; Ti cp; cp; Si cp; C; TiSi;
O*Si; SiO2; O cp

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SESSION RESUMED IN FILE 'INSPEC' AT 18:11:28 ON 17 OCT 2006
FILE 'INSPEC' ENTERED AT 18:11:28 ON 17 OCT 2006

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NEWS 1		Web Page URLs for STN Seminar Schedule - N. America
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NEWS 10	JUN 26	TULSA/TULSA2 reloaded and enhanced with new search and and display fields
NEWS 11	JUN 28	Price changes in full-text patent databases EPFULL and PCTFULL
NEWS 12	JUl 11	CHEMSAFE reloaded and enhanced
NEWS 13	JUl 14	FSTA enhanced with Japanese patents
NEWS 14	JUl 19	Coverage of Research Disclosure reinstated in DWPI
NEWS 15	AUG 09	INSPEC enhanced with 1898-1968 archive
NEWS 16	AUG 28	ADISCTI Reloaded and Enhanced
NEWS 17	AUG 30	CA(SM)/CAplus(SM) Austrian patent law changes
NEWS 18	SEP 11	CA/CAplus enhanced with more pre-1907 records
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NEWS 21	SEP 25	CAS REGISTRY(SM) no longer includes Concord 3D coordinates
NEWS 22	SEP 25	CAS REGISTRY(SM) updated with amino acid codes for pyrrolysine
NEWS 23	SEP 28	CEABA-VTB classification code fields reloaded with new classification scheme

NEWS EXPRESS	JUNE 30 CURRENT WINDOWS VERSION IS V8.01b, CURRENT MACINTOSH VERSION IS V6.0c(ENG) AND V6.0Jc(JP), AND CURRENT DISCOVER FILE IS DATED 26 JUNE 2006.
NEWS HOURS	STN Operating Hours Plus Help Desk Availability
NEWS LOGIN	Welcome Banner and News Items
NEWS IPC8	For general information regarding STN implementation of IPC 8
NEWS X25	X.25 communication option no longer available

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FILE 'HOME' ENTERED AT 18:58:48 ON 17 OCT 2006

=> **file inspec**
FILE 'INSPEC' ENTERED AT 18:58:59 ON 17 OCT 2006
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FILE LAST UPDATED: 16 OCT 2006 <20061016/UP>
FILE COVERS 1898 TO DATE.

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THE ABSTRACT (/AB), BASIC INDEX (/BI) AND TITLE (/TI) FIELDS >>>

<<< INSPEC HAS BEEN ENHANCED WITH ARCHIVE DATA 1898-1968
--> SEE NEWS
AND HELP CHANGE (last updated Aug 11, 2006) >>>

```
=> (development and titanium and applications)/ti
          114410 DEVELOPMENT/TI
           18067 TITANIUM/TI
          123073 APPLICATIONS/TI
L1             5 (DEVELOPMENT AND TITANIUM AND APPLICATIONS)/TI

=> d 1-5 ti

L1   ANSWER 1 OF 5  INSPEC  (C) 2006 IET on STN
Citing References
TI     Development of low cost titanium alloy sheets for automotive exhaust
       applications

L1   ANSWER 2 OF 5  INSPEC  (C) 2006 IET on STN
Citing References
TI     Recent research and development in titanium alloys for applications
       and healthcare goods

L1   ANSWER 3 OF 5  INSPEC  (C) 2006 IET on STN
Citing References
TI     Design and development of titanium oxide photocatalysts operating
       under visible and UV light irradiation. The applications of metal
       ion-implantation techniques to semiconducting TiO2 and Ti/zeolite
       catalysts

L1   ANSWER 4 OF 5  INSPEC  (C) 2006 IET on STN
Citing References
TI     Development and applications of titanium alloy SP-700 with high
       formability

L1   ANSWER 5 OF 5  INSPEC  (C) 2006 IET on STN
Citing References
TI     Development of the self-aligned titanium silicide process for VLSI
       applications


=> d 4,5 all

L1   ANSWER 4 OF 5  INSPEC  (C) 2006 IET on STN
Full Text  Citing References
AN     1996:5278057  INSPEC     DN  A1996-13-8140L-012
TI     Development and applications of titanium alloy SP-700 with high
       formability
AU     Ogawa, A.; Niikura, M.; Ouchi, C.;  (Mater. & Processing Res. Center, NKK
       Corp., Kawasaki, Japan), Minikawa, K.; Yamada, M.
SO     Journal of Testing and Evaluation (March 1996), vol.24, no.2, p. 100-9,
       11 refs.
       CODEN: JTEVAB, ISSN: 0090-3973
       SICI: 0090-3973(199603)24:2L.100:DATA;1-9
       Published by: ASTM, USA
DT     Journal
TC     Experimental
CY     United States
LA     English
AB     A new β-rich α+β titanium alloy SP-700, was designed to
       improve hot workability and mechanical properties over Ti-6Al-4V alloy.
       The chemical composition of the alloy is Ti-4.5Al-3V-2Mo-2Fe, and
       particularly enhance properties include superplasticity, hardenability,
       and fatigue strength. Owing to its extremely fine microstructure and low
       β-transus temperature, SP-700 is superplastically formable at
       temperatures below 1073 K without significant increase in flow stress.
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More advantageously diffusion bonding is also accomplished around this temperature. The low temperature SDF/DB process not only saves die material life and process costs, but also reduces alloy degradation from exposure at elevated temperatures, E.G. grain growth and oxidation. Isothermal and conventional hot forging are also performed better with SP-700 than ordinary titanium alloys like Ti-6Al-4V. Due to its high forgeability, SP-700 is expected to extend its application to the production of steam turbine blades. Details of practical applications have been demonstrated together with advantages of properties and fabrication for the blades

CC A8140L Deformation, plasticity and creep; A6220F Deformation and plasticity; A6220M Fatigue, brittleness, fracture, and cracks; A8140N Fatigue, embrittlement, and fracture; A8140G Other heat and thermomechanical treatments; A8140E Cold working, work hardening; post-deformation annealing, recovery and recrystallisation; textures; A8160B Surface treatment and degradation of metals and alloys; A8120G Preparation of metals and alloys (compacts, pseudoalloys)

CT bending; cold rolling; crystal microstructure; elongation; fatigue; forming processes; heat treatment; hot rolling; plastic flow; shear strength; stress corrosion cracking; superplasticity; tensile strength; titanium alloys

ST high formability; new β-rich α+β Ti-based alloy; chemical composition; superplasticity; hardenability; fatigue strength; microstructure; flow stress; Ti-Al-V

CHI TiAlV sur, Al sur, Ti sur, V sur, TiAlV ss, Al ss, Ti ss, V ss; Ti sur, Ti ss; Ti sur, Ti ss

ET Ti; Al*V; Al sy 2; sy 2; V sy 2; Al-V; AlV; Al cp; cp; V cp; Al; V; Al*Ti*V; Al sy 3; sy 3; Ti sy 3; V sy 3; TiAlV; Ti cp; Ti-6Al-4V; Al*Fe*Mo*Ti*V; Al sy 5; sy 5; Fe sy 5; Mo sy 5; Ti sy 5; V sy 5; Ti-4.5Al-3V-2Mo-2Fe

L1 ANSWER 5 OF 5 INSPEC (C) 2006 IET on STN

AN 1985:2462820 INSPEC DN B1985-034732

TI **Development** of the self-aligned **titanium** silicide process for VLSI **applications**

AU Alperin, M.E.; Hollaway, T.C.; Haken, R.A.; Gomeyer, C.D.; Karnaugh, R.V.; Parmantie, W.D. (Texas Instrum. Inc., Dallas, TX, USA)

SO IEEE Transactions on Electron Devices (Feb. 1985), vol.ED-32, no.2, p. 141-9, 19 refs.
CODEN: IETDAI, ISSN: 0018-9383
Price: 0018-9383/85/0200-0141$01.00

DT Journal

TC New Development; Practical; Experimental

CY United States

LA English

AB A manufacturable self-aligned titanium silicide process which simultaneously silicides both polysilicon gates and junctions has been developed for VLSI applications. The process produces silicided gates and junctions with sheet resistances of 1.0-2.0 Ω/square. The authors describe the application of the self-aligned titanium silicide process to NMOS VLSI circuits of the 64K SRAM class with 1-μm gate lengths. Comparison of circuit yield data and test structure parameters from devices fabricated with and without the silicidation process has demonstrated that the self-aligned silicide process is compatible with both VLSI NMOS and CMOS technologies. The self-aligned titanium silicide process has some very significant manufacturing advantages over the more conventional deposited silicide on polysilicon technologies. In particular, the problems associated with etching and depositing a polycide gate stack are eliminated with the self-aligned process since the polycide etch is replaced with a much more straightforward polysilicon only etch

CC B2550 Semiconductor device technology; B2570D CMOS integrated circuits

CT field effect integrated circuits; integrated circuit technology; semiconductor technology; silicon compounds; titanium compounds; VLSI

ST TiS2; 1 micron gate lengths; IC technology; poly-Si only etch; VLSI;

silicided gates; sheet resistances; NMOS; 64K SRAM; yield; test structure parameters; self-aligned silicide process; CMOS; manufacturing advantages; polysilicon only etch

ET S; Si; K

=>

=> d 3,22,23,24,25,27,28,32,38,47,48,55,57,59 all

L8 ANSWER 3 OF 59 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 2006:8899004 INSPEC
TI Improved ohmic contact to the n-type 4H-SiC semiconductor using cobalt silicides
AU Nam-Ihn Cho; Kyung-Hwa Jung; (Dept. of Electron. Eng., Sunmoon Univ., Asan, South Korea), Yong Choi
SO Semiconductor Science and Technology (March 2004), vol.19, no.3, p. 306-10, 12 refs.
CODEN: SSTEET, ISSN: 0268-1242
SICI: 0268-1242(200403)19:3L.306:IOCT;1-M
Price: 0268-1242/04/030306+05$30.00
Doc.No.: S0268-1242(04)68506-3
Published by: IOP Publishing, UK
DT Journal
TC Experimental
CY United Kingdom
LA English
AB Multilayer structures of cobalt and silicon have been deposited as an ohmic contact on n-type 4H-SiC substrates in order to obtain lower contact resistance and higher thermal stability. The metal structures were prepared by using electron beam evaporation on top of the silicon face of the 4H-SiC substrates, and were annealed in an atmosphere of argon with 10% hydrogen. The metal film thickness was monitored during the film deposition, and the ratio of the cobalt and silicon was fixed at 0.5 for the formation of the silicon-rich **silicide** structure (CoSi2). The electrical property of the ohmic contact has been significantly improved by the reduction of the oxide content in the metal contact layer. A **two-step annealing** process was employed to reduce oxidation problems that may occur in the heat treatment at high temperatures. The specific contact resistance of the contact structure prepared by the **two-step annealing** process was measured to decrease by more than one order of magnitude compared to that prepared by one-step annealing. The best result has been obtained as 1.8 6-10 ı ?□ cm^2 for Co/Si/Co/Si/Co metal structures after **two-step annealing**, at 500?C for 600 s and 800?C for 120 s. In the field emission scanning electron microscopy, the interface of the contact structure and SiC substrate was observed to have smooth surface morphology with CoSi2 grains
CC A7340N Electrical properties of metal-nonmetal contacts; A7340C Contact resistance, contact potential, and work functions; A6855 Thin film growth, structure, and epitaxy; A8115G Vacuum deposition; A6170A Annealing processes; A6820 Solid surface structure; B2530D Semiconductor-metal interfaces; B0520D Vacuum deposition; B2520M Other semiconductor materials; B2550A Annealing processes in semiconductor technology
CT annealing; cobalt; cobalt compounds; contact resistance; electron beam deposition; elemental semiconductors; ohmic contacts; scanning electron microscopy; semiconductor-metal boundaries; silicon; surface morphology; thermal stability; vacuum deposition
ST ohmic contact; n-type 4H-SiC semiconductor; cobalt silicides; multilayer structures; contact resistance; thermal stability; metal structures; electron beam evaporation; annealing; metal film thickness; film deposition; electrical property; heat treatment; field emission scanning electron microscopy; surface morphology; 500 degC; 800 degC; 600 s; 120 s; Co-Si-Co-Si-Co; SiC; CoSi2
CHI Co-Si-Co-Si-Co int, Co int, Si int, Co el, Si el; SiC sur, Si sur, C sur, SiC bin, Si bin, C bin; CoSi2 bin, Si2 bin, Co bin, Si bin
PHP temperature 7.73E+02 K; temperature 1.07E+03 K; time 6.0E+02 s; time 1.2E+02 s
ET C*H*Si; is; H is; 4H; SiC; Si cp; cp; C cp; 4H-SiC; Co*Si; Co sy 2; sy 2; Si sy 2; Si-Co-Si-Co; Si; Co; C; C*Si; CoSi2; Co cp

L8 ANSWER 22 OF 59 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 1997:5774385 INSPEC DN A1998-02-6822-018; B1998-01-2550F-064
TI TiSi2 phase transformation by amorphization techniques
AU Karlin, T.; Samuelsson, M.; (Solid State Electron., R. Inst. of Technol., Stockholm, Sweden), Nygren, S.; Ostling, M.
SO Thin Films - Structure and Morphology. Symposium, 1997, p. 283-8 of xvii+793 pp., 9 refs.
Editor(s): Moss, S.C.; Ila, D.; Cammarata, R.C.; Chason, E.H.; Einstein, T.L.; Williams, E.D.
Published by: Mater. Res. Soc, Pittsburgh, PA, USA
Conference: Thin Films - Structure and Morphology. Symposium, Boston, MA, USA, 2-6 Dec. 1996
DT Conference; Conference Article
TC Application; Experimental
CY United States
LA English
AB ULSI packing density calls for sub-micron line widths, but on n-type polysilicon this can lead to incomplete titanium **silicide** C49 to C54 phase transformation after a conventional **two step** rapid thermal **anneal** (RTA). This study compares three different ion beam amorphization techniques: preamorphization, ion beam mixing and **silicide** amorphization, aiming at a complete phase transformation for submicron **silicide** lines. For preamorphization, an arsenic implantation at moderate energies (35-75 keV) was used to amorphize the top layer of the polysilicon prior to the titanium deposition. Ion beam mixing used a high-energy (200 keV) arsenic implantation after the titanium deposition to create an amorphous mix of silicon and titanium. These two methods did, each by themselves, lead to an increased fraction of C54 **silicide** grains already during the low temperature RTA, and a complete phase transformation during the subsequent high temperature RTA. Both methods lowered the thickness difference between titanium **silicide** on p- and n-type silicon. **Silicide** amorphization with 75 keV arsenic or 100 keV antimony, applied before the second RTA, did not significantly improve the **silicide** phase transformation
CC A6822 Surface diffusion, segregation and interfacial compound formation; A6140 Structure of amorphous and polymeric materials; A6180J Ion beam effects; A6630N Chemical interdiffusion in solids; A6470K Solid-solid transitions; A8130H Constant-composition solid-solid phase transformations: polymorphic, massive, and order-disorder; A6170T Doping and implantation of impurities; A7340N Electrical properties of metal-nonmetal contacts; A6170A Annealing processes; B2550F Metallisation and interconnection technology; B2570 Semiconductor integrated circuits; B2550A Annealing processes in semiconductor technology; B2550B Semiconductor doping; B2530D Semiconductor-metal interfaces
CT amorphisation; integrated circuit metallisation; ion beam applications; ion beam mixing; ion implantation; rapid thermal annealing; semiconductor doping; semiconductor-metal boundaries; solid-state phase transformations; titanium compounds; ULSI
ST TiSi2 phase transformation; amorphization techniques; ULSI packing density; sub-micron line widths; n-type polysilicon; C49 to C54 phase transformation; rapid thermal anneal; ion beam amorphization techniques; preamorphization; ion beam mixing; silicide amorphization; complete phase transformation; submicron silicide lines; As implantation; Ti deposition; C54 silicide grains; 35 to 75 keV; 200 keV; 100 keV; TiSi2; Si; Ti; Si:As; Si:Sb
CHI TiSi2 int, Si2 int, Si int, Ti int, TiSi2 bin, Si2 bin, Si bin, Ti bin; Si sur, Si el; Ti int, Ti el; Si int, Si el; Si:As int, As int, Si int, Si:As bin, As bin, Si bin, As el, Si el, As dop; Si:Sb int, Sb int, Si int, Si:Sb bin, Sb bin, Si bin, Sb el, Si el, Sb dop
PHP electron volt energy 3.5E+04 to 7.5E+04 eV; electron volt energy 2.0E+05 eV; electron volt energy 1.0E+05 eV
ET Si2; C; Si; Ti; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi; Ti cp; cp; Si cp; As; As*Si; As sy 2; Si:As; As doping; doped materials; Sb; Sb*Si; Sb sy 2; Si:Sb; Sb doping

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Full Text | Citing References

AN 1996:5453976 INSPEC DN B1997-02-2550F-006
TI Formation of Ti-silicides by rapid thermal annealing
AU Ohm, W.Y.; Chang, H.J.; Chang, G.K.; (Dept. of Electr. Eng., Dankook Univ., South Korea), Song, J.T.
SO Journal of the Korean Institute of Telematics and Electronics (Aug. 1996), vol.33A, no.8, p. 125-31, 10 refs.
CODEN: CKNOEZ, ISSN: 1016-135X
SICI: 1016-135X(199608)33A:8L.125:FSRT;1-N
Published by: Korea Inst. Telematics & Electron, South Korea
DT Journal
TC Practical; Experimental
CY Korea, Democratic Peoples Republic of
LA Korean
AB The substrates, n-type (100) Si wafers, are subjected to standard cleaning procedures followed by a diluted HF solution dip immediately prior to loading into the e-beam chamber. Thin Ti films with a thickness of 1000 A are deposited by e-beam evaporation with a base pressure of 46-10ı torr. Ti-silicidations from Ti(1000 A)/Si samples are performed in a RTA system by direct **annealing** and **two step annealing** over a range of temperatures (T=450 850?C) and times (t=5 60 sec) in an atmosphere of N2 and Ar. The sheet resistance of Ti-silicides obtained by direct annealing depends on RTA process variables such as temperatures, times and gas ambiences at annealing temperatures below 600?C, while showing a nearly constant value (0.8?□/.box.d"Rsd"1.2?□/.box.) above 700?C.
The sheet resistance of TiSi2(C54) prepared by **two step annealing** (first **annealing** step at 600?C, second annealing step at 800?C for 20 sec) depends on the first annealing time due to the variation of Ti-**silicide** thickness. TEM micrographs and XRD analyses exhibit that the resistivity and the crystallinity of TiSi2(C54) are about 20 ?□/?□cm and (040)-orientation, respectively
CC B2550F Metallisation and interconnection technology; B2570 Semiconductor integrated circuits; B2550A Annealing processes in semiconductor technology; B0170E Production facilities and engineering; B2550E Surface treatment (semiconductor technology); B0520F Chemical vapour deposition; E1520N Surface treatment and coating techniques
CT electric resistance; electrical resistivity; electron beam deposition; integrated circuit interconnections; integrated circuit metallisation; rapid thermal annealing; surface cleaning; titanium compounds; transmission electron microscopy; X-ray diffraction
ST Ti-silicide formation; rapid thermal annealing; n-type Si wafers; standard cleaning procedures; diluted HF solution dip; e-beam chamber; thin Ti films; e-beam evaporation; TEM micrographs; Ti-silicidations; Ti-Si samples; direct annealing; two step annealing; N2-Ar atmosphere; sheet resistance; XRD analysis; RTA process variables; RTA temperature; RTA time; RTA gas ambience; annealing temperatures; TiSi2; 1000 angstrom; 0.004 mtorr; 450 to 850 C; 5 to 60 s; 600 C; 700 C; 800 C; 20 s; 20 muohmcm; Si; Ti-Si; TiSi2-Si; HF; N2-Ar
CHI Si sur, Si el; Ti-Si int, Si int, Ti int, Si el, Ti el; TiSi2-Si int, TiSi2 int, Si2 int, Si int, Ti int, TiSi2 bin, Si2 bin, Si bin, Ti bin, Si el; HF bin, F bin, H bin; N2Ar bin, Ar bin, N2 bin, N bin
PHP size 1.0E-07 m; pressure 5.3E-04 Pa; temperature 7.23E+02 to 1.12E+03 K; time 5.0E+00 to 6.0E+01 s; temperature 8.73E+02 K; temperature 9.73E+02 K; temperature 1.07E+03 K; time 2.0E+01 s; resistivity 2.0E-07 ohm*m
ET Si; F*H; HF; H cp; cp; F cp; Ti; Ar; Si2-Si; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi; Ti cp; Si cp; N; C; N2; C*Si*Ti; C sy 3; sy 3; Si sy 3; Ti sy 3; TiSi2(C; C cp

L8 ANSWER 24 OF 59 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 1996:5450452 INSPEC DN B1997-01-2530D-041
TI Low ohmic cobalt **silicide** contacts to p-type 6H-SiC
AU Ostling, M.; Lundberg, N. (Dept. of Electron., R. Inst. of Technol., Stockholm, Sweden)
SO 1996. 54th Annual Device Research Conference Digest (Cat. No.96TH8193),

1996, p. 157 of 202 pp., 8 refs.
ISBN: 0 7803 3358 6
Published by: IEEE, New York, NY, USA
Conference: 1996 54th Annual Device Research Conference Digest, Santa Barbara, CA, USA, 24-26 June 1996
Sponsor(s): IEEE Electron Devices Soc

DT Conference; Conference Article
TC Experimental
CY United States
LA English

AB Summary form only given, as follows. Thermally stable ohmic contacts with low specific contact resistivities is one of the key issues that needs to be addressed to enable successful fabrication of SiC power devices for commercial applications. Recent advances in epilayer growth provides highly Al-doped p-type layers which form the basis for low ohmic contacts. Most of the earlier reported ohmic contacts to p-type 6H-SiC have used Al-based metallizations yielding resistivities approximately in the 10-4-10-5 ?□cm^2 range but with poor thermal stability. The lowest resistivities were usually achieved after a burn-in around 800-1000?C and further annealing at higher temperatures or for extended time decayed the ohmic properties. However, refractory metal silicides with their low resistivity, thermal stability and overall manufacturability look promising as contact materials to SiC for high temperature operation. In this study thermally stable CoSi2 ohmic contacts to p-type 6H-SiC possessing low specific contact resistivity in the mid 10-6 cm^2 region are reported. TLM structures were fabricated on a 1 ?□m thick Si-face Al-doped epilayer on top of an n-type substrate through a sequential electron beam evaporation of Co and Si layers followed by a **two step** vacuum **annealing** process at 500?C and 900?C. The specific contact resistivity is investigated as a function of operating temperature (20-200?C), current density and ageing at 1100?C in a vacuum furnace

CC B2530D Semiconductor-metal interfaces; B0520F Chemical vapour deposition
CT ageing; annealing; cobalt compounds; contact resistance; current density; electron beam deposition; ohmic contacts; power semiconductor devices; semiconductor-metal boundaries; silicon compounds; thermal stability; vacuum deposited coatings; wide band gap semiconductors
ST low ohmic contacts; p-type 6H-SiC; thermally stable ohmic contacts; specific contact resistivities; SiC power devices; epilayer growth; Al-doped p-type layers; refractory metal silicides; high temperature operation; CoSi2 ohmic contacts; n-type substrate; sequential electron beam evaporation; two step vacuum annealing process; current density; ageing; 20 to 200 C; 500 C; 900 C; 1100 C; CoSi2-SiC
CHI CoSi2-SiC int, CoSi2 int, Si2 int, SiC int, Co int, Si int, C int, CoSi2 bin, Si2 bin, SiC bin, Co bin, Si bin, C bin
PHP temperature 2.93E+02 to 4.73E+02 K; temperature 7.73E+02 K; temperature 1.17E+03 K; temperature 1.37E+03 K
ET C*H*Si; is; H is; 6H; SiC; Si cp; cp; C cp; 6H-SiC; C; Si2; C*Si; C sy 2; sy 2; Si sy 2; Si2-SiC; Si; Co*Si; Co sy 2; CoSi; Co cp; Co; Al; CoSi2

L8 ANSWER 25 OF 59 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 1996:5442232 INSPEC DN B1997-01-2530D-032
TI Thermally stable low ohmic contacts to p-type 6H-SiC using cobalt silicides
AU Lundberg, N.; Ostling, M. (Dept. of Electron., R. Inst. of Technol., Stockholm, Sweden)
SO Solid-State Electronics (Nov. 1996), vol.39, no.11, p. 1559-65, 22 refs.
CODEN: SSELA5, ISSN: 0038-1101
SICI: 0038-1101(199611)39:11L.1559:TSOC;1-6
Price: 0038-1101/96/$15.00+0.00
Doc.No.: S0038-1101(96)00071-8
Published by: Elsevier, UK

DT Journal
TC Experimental
CY United Kingdom

LA English
AB Cobalt **silicide** (CoSi2) ohmic contacts possessing low specific contact resistivity (?c<4.0?0.76-10ı ?□ cm^2) to p-type 6H-SiC are reported. The contacts were fabricated through sequential electron-beam evaporation of Co and Si layers forming a Si/Co/SiC structure, followed by a two-**step** **vacuum** annealing **process** at 500 and 900?C, respectively. Specific contact resistivities were extracted from transmission line model (TLM) structures at temperatures ranging from 22 to 200?C. ?c is investigated as a function of current density, temperature and ageing in a vacuum furnace at 1100?C. Furthermore, comparison with a Co/SiC contact structure subjected to an identical annealing process revealed higher ?c and a modified sheet resistance requiring a different method of contact parameter extraction
CC B2530D Semiconductor-metal interfaces; B2550A Annealing processes in semiconductor technology; B0520F Chemical vapour deposition; B2520M Other semiconductor materials
CT annealing; cobalt compounds; contact resistance; electron beam deposition; ohmic contacts; silicon compounds; thermal stability; wide band gap semiconductors
ST thermal stability; ohmic contact; p-type 6H-SiC; cobalt silicide; specific contact resistivity; electron-beam evaporation; vacuum annealing; transmission line model; sheet resistance; parameter extraction; 500 to 900 C; 22 to 200 C; 1100 C; SiC-CoSi2
CHI SiC-CoSi2 int, CoSi2 int, Si2 int, SiC int, Co int, Si int, C int, CoSi2 bin, Si2 bin, SiC bin, Co bin, Si bin, C bin
PHP temperature 7.73E+02 to 1.17E+03 K; temperature 2.95E+02 to 4.73E+02 K; temperature 1.37E+03 K
ET C*H*Si; is; H is; 6H; SiC; Si cp; cp; C cp; 6H-SiC; C*Co*Si; C sy 3; sy 3; Co sy 3; Si sy 3; CoSi2; Co cp; C-CoSi2; CoSi; C-CoSi; Co*Si; Co sy 2; sy 2; Si sy 2; Si; C*Si; Co; C

L8 ANSWER 27 OF 59 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 1996:5225908 INSPEC DN B1996-05-2550A-006
TI In-situ resistance measurements during rapid thermal annealing for process characterization
AU Colgan, E.G.; Cabral, C. Jr.; Clevenger, L.A.; (Microelectron. Div., IBM Corp., East Fishkill, NY, USA), Harper, J.M.E.
SO Rapid Thermal and Integrated Processing IV. Symposium, 1995, p. 49-54 of xii+454 pp., 21 refs.
Editor(s): Brueck, S.R.J.; Gelpey, J.C.; Kermani, A.; Regolini, J.L.; Sturm, J.C.
Published by: Mater. Res. Soc, Pittsburgh, PA, USA
Conference: Rapid Thermal and Integrated Processing IV. Symposium, San Francisco, CA, USA, 17-20 April 1995
DT Conference; Conference Article
TC Practical; Experimental
CY United States
LA English
AB Measurement of resistance in-situ during rapid thermal annealing is a powerful technique for process characterization and optimization. A major advantage of in-situ resistance measurements is the very rapid process learning. With silicides, in-situ resistance measurements can quickly determine an appropriate thermal process in which a low resistance **silicide** phase is formed without the agglomeration or inversion of **silicide**/polycrystalline silicon structures. One example is an optimized **two** **step** **anneal** for CoSi2 formation which was developed in less than one day. Examples of process characterization include determining the phase formation kinetics of TiSi2 (C49 and C54), Co2Si, and CoSi2 using in-situ ramped resistance measurements. The stability of TiSi2 or CoSi2/poly-Si structures has also been characterized by isothermal measurements. Resistance measurements have been made at heating rates from 1 to 100?C/s and temperatures up to 1000?C. The sample temperature was calibrated by melting AgSi, AlSi, or AuSi eutectics

CC B2550A Annealing processes in semiconductor technology; B7310J Impedance and admittance measurement; B2570 Semiconductor integrated circuits; B7130 Measurement standards and calibration; B7320R Thermal variables measurement

CT calibration; cobalt compounds; electric resistance measurement; integrated circuit technology; optimisation; rapid thermal annealing; temperature measurement; thermal stability; titanium compounds

ST in-situ resistance measurement; rapid thermal annealing; process characterization; process optimization; process learning; AgSi eutectic; low resistance silicide phase formation; agglomeration; structure inversion; silicide/polycrystalline silicon structures; optimized two step anneal; CoSi2 formation; phase formation kinetics; TiSi2 formation; Co2Si formation; AlSi eutectic; in-situ ramped resistance measurement; TiSi2/poly-Si structures; CoSi2/poly-Si structures; isothermal measurement; AuSi eutectic; sample temperature calibration; 1000 C; Ti-Si; TiSi2-Si; Co-Si; CoSi2-Si; Co2Si-Si; AgSi; AlSi; AuSi

CHI Ti-Si int, Si int, Ti int, Si el, Ti el; TiSi2-Si int, TiSi2 int, Si2 int, Si int, Ti int, TiSi2 bin, Si2 bin, Si bin, Ti bin, Si el; Co-Si int, Co int, Si int, Co el, Si el; CoSi2-Si int, CoSi2 int, Si2 int, Co int, Si int, CoSi2 bin, Si2 bin, Co bin, Si bin, Si el; Co2Si-Si int, Co2Si int, Co2 int, Co int, Si int, Co2Si bin, Co2 bin, Co bin, Si bin, Si el; AgSi bin, Ag bin, Si bin; AlSi bin, Al bin, Si bin; AuSi bin, Au bin, Si bin

PHP temperature 1.27E+03 K

ET Si; Si2; Si2-Si; Si-Si; Ti; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi; Ti cp; cp; Si cp; Co; Co*Si; Co sy 2; CoSi; Co cp; Co2Si; Ag; Al; Au; CoSi2; TiSi2; C; Ag*Si; Ag sy 2; AgSi; Ag cp; Al*Si; Al sy 2; AlSi; Al cp; Au*Si; Au sy 2; AuSi; Au cp

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Full Text | Citing References

AN 1996:5177443 INSPEC DN A1996-05-6170A-008; B1996-03-2550A-013

TI In-situ resistance measurements during rapid thermal annealing for process characterization

AU Colgan, E.G.; Cabral, C. Jr.; Clevenger, L.A.; (IBM Microelectron. Div., East Fishkill, NY, USA), Harper, J.M.E.

SO Modeling and Simulation of Thin-Film Processing. Symposium, 1995, p. 321-6 of xi+382 pp., 21 refs.
Editor(s): Srolovitz, D.J.; Volkert, C.A.; Fluss, M.J.; Kee, R.J.
Published by: Mater. Res. Soc, Pittsburgh, PA, USA
Conference: Modeling and Simulation of Thin-Film Processing. Symposium, San Francisco, CA, USA, 17-20 April 1995

DT Conference; Conference Article

TC Experimental

CY United States

LA English

AB Measurement of resistance in-situ during rapid thermal annealing is a powerful technique for process characterization and optimization. A major advantage of in-situ resistance measurements is the very rapid process learning. With silicides, in-situ resistance measurements can quickly determine an appropriate thermal process in which a low resistance **silicide** phase is formed without the agglomeration or inversion of **silicide**-polycrystalline silicon structures. One example is an optimized **two step anneal** for CoSi2 formation which was developed in less than one day. Examples of process characterization include determining the phase formation kinetics of TiSi2 (C49 and C54), Co2Si and CoSi2 using in-situ ramped resistance measurements. The stability of TiSi2 or CoSi2/poly-Si structures has also been characterized by isothermal measurements. Resistance measurements have been made at heating rates from 1 to 100?C/s and temperatures up to 1000?C. The sample temperature was calibrated by melting Ag,Al or Au/Si eutectics

CC A6170A Annealing processes; A7320A Surface states, band structure, electron density of states; A7340N Electrical properties of metal-nonmetal contacts; B2550A Annealing processes in semiconductor technology; B2520C Elemental semiconductors; B2530D Semiconductor-metal

interfaces
CT cobalt compounds; electrical resistivity; elemental semiconductors; rapid thermal annealing; semiconductor-metal boundaries; silicon; titanium compounds
ST resistance; rapid thermal annealing; rapid process learning; two step anneal; phase formation kinetics; isothermal measurements; heating rates; melting; 1000 degC; TiSi2-Si; CoSi2-Si
CHI TiSi2-Si int, TiSi2 int, Si2 int, Si int, Ti int, TiSi2 bin, Si2 bin, Si bin, Ti bin, Si el; CoSi2-Si int, CoSi2 int, Si2 int, Co int, Si int, CoSi2 bin, Si2 bin, Co bin, Si bin, Si el
PHP temperature 1.27E+03 K
ET Si2-Si; Si; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi; Ti cp; cp; Si cp; Ti; Co*Si; Co sy 2; CoSi; Co cp; Co; CoSi2; TiSi2; C; Co2Si; Ag; Al; Au

L8 ANSWER 32 OF 59 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 1995:4849385 INSPEC DN A1995-03-6822-003
TI Interdiffusion, phase transformation, and epitaxial CoSi2 formation in multilayer Co/Ti-Si(100) system
AU Feng Hong; Rozgonyi, G.A. (Dept. of Mater. Sci. & Eng., North Carolina State Univ., Raleigh, NC, USA)
SO Journal of the Electrochemical Society (Dec. 1994), vol.141, no.12, p. 3480-8, 31 refs.
CODEN: JESOAN, ISSN: 0013-4651
Price: 0013-4651/94/$5.00+0.00
DT Journal
TC Experimental
CY United States
LA English
AB Interdiffusion, phase transformation, and epitaxial CoSi2 formation in a Co/Ti multilayer-Si(100) system have been investigated. Evaporated and sputtered Co/Ti multilayers were deposited on RCA-cleaned and dilute HF-dipped Si(100) substrate. The multilayer system was then subsequently heat-treated by a **two-step annealing** process. An initial Ti(O) amorphous layer formed due to oxygen/carbon incorporation during the deposition, or a TiSix amorphous layer formed by solid-state amorphization reaction. These interfacial layers evolved into a Co-Ti(O)-Si amorphous alloy which functioned as a diffusion membrane which controlled the phase formed during subsequent annealing. The Co-**silicide** phase sequence was CoSi2?!Co2Si?!CoSi, and finally CoSi2 from 550?C to higher temperature. Preferentially oriented (311) CoSi formed as the dominant phase in the temperature range from 650 to 800?C. Epitaxial CoSi, nucleated from the CoSi template layer and grew substantially during the high temperature second annealing. The resulting epitaxial CoSi2 layer exhibited superior thermal stability and a resistivity as low as 15 ?□?□-cm, even for nanoscale thicknesses. Interface impurity cleansing by Ti, uniform and slow Co supply through the interfacial amorphous membrane, and a positive effect of the capping layers throughout the process promoted preferential (311) CoSi formation and subsequent epitaxial CoSi2 growth
CC A6822 Surface diffusion, segregation and interfacial compound formation; A6630N Chemical interdiffusion in solids; A6855 Thin film growth, structure, and epitaxy; A8140G Other heat and thermomechanical treatments; A6140 Structure of amorphous and polymeric materials; A6842 Surface phase transitions and critical phenomena
CT amorphisation; annealing; chemical interdiffusion; cobalt; electrical resistivity; epitaxial layers; metallic superlattices; nanostructured materials; sputtered coatings; surface diffusion; surface phase transformations; thermal stability; titanium
ST Co/Ti-Si(100); phase transformation; CoSi2; interdiffusion; RCA-cleaned substrate; dilute HF-dipped substrate; annealing; amorphization; diffusion membrane; thermal stability; resistivity; nanoscale thicknesses; interface impurity cleansing; 550 to 800 C; Si; Co-Ti-Si
CHI Si sur, Si el; Co-Ti-Si int, Co int, Si int, Ti int, Co el, Si el, Ti el; CoSi2 bin, Si2 bin, Co bin, Si bin
PHP temperature 8.23E+02 to 1.07E+03 K

ET Si*Ti; Si sy 2; sy 2; Ti sy 2; Ti-Si; Si; F*H; HF; H cp; cp; F cp; Co; Ti; Co*Si; Co sy 2; CoSi2; Co cp; Si cp; TiSix; Ti cp; Co*O*Si*Ti; Co sy 4; sy 4; O sy 4; Si sy 4; Ti sy 4; Ti(O); O cp; Co-Ti(O)-Si; Co2Si; CoSi; C

L8 ANSWER 38 OF 59 INSPEC (C) 2006 IET on STN

Full Text | Citing References

AN 1991:3989701 INSPEC DN B1991-069454

TI Formation of cobalt **silicide** under a passivating film of molybdenum or tungsten

AU Fann-Mei Yang; Mao-Chieh Chen (Dept. of Electron. Eng., Nat. Chiao Tung Univ., Hsinchu, Taiwan)

SO Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena) (May-June 1991), vol.9, no.3, p. 1497-502, 12 refs.
CODEN: JVTBD9, ISSN: 0734-211X
Price: 0734-211X/91/031497-06$01.00

DT Journal

TC New Development; Practical; Experimental

CY United States

LA English

AB A very simple and reproducible cobalt **silicide** process with Mo/Co or W/Co bilayer metallization to overcome the oxidizing liability of Co annealed in a normal flowing-nitrogen furnace has been developed. Cobalt is deposited on blank and patterned silicon wafers in an electron-beam evaporation system followed by Mo (or W) deposition without breaking the vacuum. The cobalt silicidation is carried out using a **two-step annealing** process. The first **annealing** is performed at a temperature ranging from 400 to 600?C, during which the role of the upper layer of Mo (or W) is to protect the underlying Co layer from being oxidized while not disturbing the cobalt's silicidation process. Perfect selective etching of Mo (or W) can be accomplished by a NH4OH+H2O2+(2-3)H2O solution. The second annealing is performed at a higher temperature of 750?C to completely transform the CoSi obtained in the first annealing into CoSi2 and induce grain growth of CoSi2, thus lowering the resistivity X-ray diffraction, Auger electron spectroscopy, scanning electron microscopy, and sheet resistance measurement are used to characterize the **silicide** phase and microstructure

CC B2550F Metallisation and interconnection technology; B2570 Semiconductor integrated circuits; B2550E Surface treatment (semiconductor technology)

CT cobalt compounds; integrated circuit technology; metallisation; molybdenum; tungsten; VLSI

ST reproducible silicidation process; wet etching; reliable method; cobalt silicidation; two-step annealing process; selective etching; X-ray diffraction; Auger electron spectroscopy; scanning electron microscopy; sheet resistance measurement; microstructure; 400 to 600 degC; 750 degC; NH4OH-H2O2-H2O etch solution; Mo passivating film; CoSi2 formation; W passivating film; Mo-Co bilayer metallisation; W-Co bilayer metallisation

CHI NH4OHH2O2H2O ss, H2 ss, H4 ss, O2 ss, OH ss, H ss, N ss, O ss; Mo el; CoSi2 bin, Si2 bin, Co bin, Si bin; W el; MoCo bin, Co bin, Mo bin; WCo bin, Co bin, W bin

PHP temperature 6.73E+02 to 8.73E+02 K; temperature 1.02E+03 K

ET H*O; OH; O cp; cp; H cp; H2O2; H2O; OH-H2O2-H2O; Si2; Co; O2H2O; H; O; Si; Mo; W; C; H*N*O; NH4OH; N cp; NH4OH+H2O2; Co*Si; Co sy 2; sy 2; Si sy 2; CoSi; Co cp; Si cp; CoSi2

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AN 1989:3279046 INSPEC DN A1989-009152

TI Deposition and properties of plasma-enhanced CVD titanium **silicide**

AU Hara, T.; Ishizawa, Y.; Hung Ming Wu; (Dept. of Electr. Eng., Hosei Univ., Tokyo, Japan), Hemmes, D.G.; Rosler, R.S.

SO Proceedings of the Tenth International Conference on Chemical Vapor Deposition 1987, 1987, p. 867-76 of xvi+1269 pp., 7 refs.
Editor(s): Cullen, G.W.; Blocher, J.M. Jr.
Published by: Electrochem. Soc, Pennington, NJ, USA

Conference: Proceedings of the Tenth International Conference on Chemical Vapor Deposition 1987, Honolulu, HI, USA, Oct. 1987
Sponsor(s): Electrochem. Soc. Japan; Japan Soc. Appl. Phys
DT Conference; Conference Article
TC Experimental
CY United States
LA English
AB Titanium **silicide** layers with different silicon compositions, x, are deposited by plasma-enhanced chemical vapor deposition. The composition can be changed from 1.1 to 2.0 with varying TiCl4/SiH4 gas flow rate ratio from 0.23 to 0.09. Sheet resistance of as-deposited layers decreases with increasing silicon composition and reached 5.0 Ohm/sq in TiSi layers. Sheet resistance decreases to 1.8 Ohm/sq with increasing annealing temperature. This minimum value can be achieved when TiSi2 is formed, for instance, at 600 and 700?C in TiSi1.1 and TiSi1.8, respectively. Interfacial reaction of a multi-layer structure consisting of Si(1000 A)/TiSix(1200 A)/Si(700 A) is studied. When one-step annealing is performed at 1000?C, a rough TiSix/Si interface and an increase of sheet resistance appear. However a stable interface can be attained at the interface and sheet resistance remain stable using a **two-step** rapid thermal **anneal** for PECVD TiSix: pre-anneal at 700?C and post-anneal at 1000?C. Pre-anneals at 600 and 800?C result in an inhomogeneous interface in the post-**anneal** at 1000?C. **Two-step annealing** with a pre-**anneal** at 700?C in PECVD TiSix is a promising process technology for VLSI's
CC A8115H Chemical vapour deposition; A6855 Thin film growth, structure, and epitaxy; A7360D Electrical properties of metals and metallic alloys (thin films/low-dimensional structures); A6822 Surface diffusion, segregation and interfacial compound formation
CT annealing; electronic conduction in metallic thin films; plasma CVD; titanium compounds
ST sheet resistance; interfacial reaction; plasma-enhanced CVD; composition; annealing temperature; multi-layer structure; two-step rapid thermal anneal; pre-anneal; post-anneal; TiSi2; TiSi1.1; TiSi1.8; TiCl4-SiH4; TiSix-Si; TiCl4; SiH4
CHI TiCl4SiH4 ss, Cl4 ss, Cl ss, H4 ss, Si ss, Ti ss, H ss; TiSi-Si int, TiSi int, Si int, Ti int, TiSi bin, Si bin, Ti bin, Si el; TiCl4 bin, Cl4 bin, Cl bin, Ti bin; SiH4 bin, H4 bin, Si bin, H bin; TiSi2 bin, Si2 bin, Si bin, Ti bin; TiSi1.1 bin, Si1.1 bin, Si bin, Ti bin; TiSi1.8 bin, Si1.8 bin, Si bin, Ti bin
ET Si; Cl*H*Si; SiH4; Si cp; cp; H cp; Cl4-SiH4; Six-Si; Cl; Cl4SiH; Cl cp; H; Ti; Si-Si; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi; Ti cp; Cl*Ti; TiCl4; H*Si; TiSi2; C; TiSi1.1; TiSi1.8; TiSix

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AN 1988:3138639 INSPEC DN A1988-070242
TI High temperature stability of plasma-enhanced chemically vapour deposited titanium **silicide** due to **two-step** rapid thermal **annealing**
AU Hara, T.; Ishizawa, Y.; (Dept. of Electr. Eng., Hosei Univ., Tokyo, Japan), Hemmes, D.G.; Rosler, R.S.
SO Thin Solid Films (15 Feb. 1988), vol.157, no.1, p. 135-72, 9 refs.
CODEN: THSFAP, ISSN: 0040-6090
Price: 0040-6090/88/$3.50
DT Journal
TC Experimental
CY Switzerland
LA English
AB The high temperature stability of plasma-enhanced chemically vapour deposited titanium **silicide** (TiSix) annealed at 1000?C is studied. A multilayer structure consisting of Si(1000 A)/TiSix(1200 A)/Si(700 A) is deposited successively over thermal oxide on a silicon substrate. When one-step rapid thermal annealing is performed at 1000?C, a rough TiSix-Si interface forms and an increase in sheet resistance occurs. However, a stable interface and sheet resistance can be attained using a two-step rapid thermal sequence consisting of a

700?C pre-anneal and 1000?C post-anneal owing to the fact that stoichiometric TiSix possessing an even TiSix-Si interface is formed with this pre-anneal. Pre-anneals at 600 and 800?C result in an inhomogeneous interface when followed by the post-**anneal** at 1000?C. **Two-step annealing** with a 700?C pre-anneal is a promising process technology for very large scale integrated circuit fabrication

CC A6822 Surface diffusion, segregation and interfacial compound formation; A6855 Thin film growth, structure, and epitaxy; A8115H Chemical vapour deposition; A8140G Other heat and thermomechanical treatments

CT annealing; CVD coatings; interface structure; titanium compounds

ST plasma-enhanced; high temperature stability; rapid thermal annealing; TiSix-Si interface; sheet resistance; very large scale integrated circuit fabrication; TiSix

CHI TiSi bin, Si bin, Ti bin

ET Six-Si; Si; Ti; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSix; Ti cp; cp; Si cp; C; TiSix-Si

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AN 1986:2645522 INSPEC DN A1986-052199

TI Formation of smooth CoSi2 films by solid phase epitaxy

AU Furukawa, S.; Ishibashi, K. (Graduate Sch. of Sci. & Eng., Tokyo Inst. of Technol., Yokohama, Japan)

SO Layered Structures and Interface Kinetics: Their Technology and Applications. US-Japan Seminar on `Solid Phase Epitaxy and Interface Kinetics', 1985, p. 187-97 of viii+369 pp., 10 refs.
Editor(s): Furukawa, S.
ISBN: 90 277 1939 X
Published by: Reidel, Dordrecht, Netherlands
Conference: Layered Structures and Interface Kinetics: Their Technology and Applications. US-Japan Seminar on `Solid Phase Epitaxy and Interface Kinetics', Oiso, Japan, 20-24 June 1983
Sponsor(s): NSF; Japan Soc. Promotion Sci

DT Conference; Conference Article

TC Experimental

CY Netherlands

LA English

AB Formation of CoSi2 film by solid-phase epitaxy is investigated by Rutherford backscattering spectroscopy and scanning electron microscopy. When the **silicide** is formed by a conventional SPE process, the film is not usually uniform and the surface of the sample consists of both Si areas and formed CoSi2 areas. **Two step annealing** process proposed is effective to improve not only the uniformity of the film, e.g. the Si areas are drastically decreased, but also the crystallinity of the film. Patterning of a surface of a Si wafer in the form of stripes or squares before **silicide** growth is also effective to improve the uniformity of the film. The growth kinetics of the **silicide** in the case of conventional process and **two step annealing** process are also discussed by observing the initial stages of the **silicide** formation

CC A6855 Thin film growth, structure, and epitaxy; A8115 Methods of thin film deposition; A8140G Other heat and thermomechanical treatments

CT annealing; cobalt alloys; epitaxial growth; metallic epitaxial layers; particle backscattering; scanning electron microscope examination of materials; silicon alloys

ST CoSi2 films; solid phase epitaxy; Rutherford backscattering spectroscopy; scanning electron microscopy; annealing; crystallinity

ET Si2; Co*Si; Co sy 2; sy 2; Si sy 2; CoSi2; Co cp; cp; Si cp; Si

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AN 1985:2514279 INSPEC DN A1985-101677; B1985-050272

TI Titanium silicidation by halogen lamp annealing

AU Okamoto, T.; Tsukamoto, K.; Shimizu, M.; Matsukawa, T. (LSI Res. & Dev. Lab., Mitsubishi Electr. Corp., Itami, Japan)

SO Journal of Applied Physics (15 June 1985), vol.57, no.12, p. 5251-5, 15

refs.
CODEN: JAPIAU, ISSN: 0021-8979
Price: 0021-8979/85/125251-05$02.40
DT Journal
TC Experimental
CY United States
LA English
AB Silicidation of titanium (Ti) thin films sputter-deposited onto silicon (Si) was performed by the halogen lamp annealing method. This method was found to be quite effective in forming oxide-free and homogeneous titanium disilicide (TiSi2). Temperature dependence of silicidation was investigated by using Rutherford backscattering spectroscopy, X-ray diffraction, and sheet resistance measurements. It was found that the dominant crystal phase of **silicide** formed during annealing at 600 and 625?C for 90 sec was titanium monosilicide (TiSi), and that a homogeneous TiSi2 with resistivity of 15 ?□?□ cm was formed at 700?C. Self-aligned TiSi2 with low resistivity can be obtained with **two-step annealing**: the first-step **annealing** was carried out below 600?C and followed by removal of unreacted Ti on silicon dioxide (SiO2), and the second-step annealing was carried out above 650?C
CC A6180 Radiation damage and other irradiation effects; A6180 Radiation damage and other irradiation effects; A6630N Chemical interdiffusion in solids; A6848 Solid-solid interfaces; A7360D Electrical properties of metals and metallic alloys (thin films/low-dimensional structures); A7920N Atom-, molecule-, and ion-surface impact and interactions; B2530D Semiconductor-metal interfaces; B2550F Metallisation and interconnection technology
CT diffusion in solids; electronic conduction in metallic thin films; incoherent light annealing; interface structure; metallic thin films; metallisation; particle backscattering; semiconductor-metal boundaries; sputtered coatings; titanium; titanium compounds; X-ray diffraction examination of materials
ST TiSi; Ti silicidation; Ti sputter deposited thin films; temperature dependence; halogen lamp annealing; Rutherford backscattering spectroscopy; X-ray diffraction; sheet resistance measurements; dominant crystal phase; TiSi2; two-step annealing
ET Si; Ti; Si*Ti; Si sy 2; sy 2; Ti sy 2; TiSi2; Ti cp; cp; Si cp; C; TiSi; O*Si; SiO2; O cp

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AN 1984:2295351 INSPEC DN A1984-084537; B1984-041066
TI Study on formation of solid-phase-epitaxial CoSi2 films and patterning effects
AU Ishibashi, K.; Ishiwara, H.; Furukawa, S. (Graduate School of Sci. & Engng., Tokyo Inst. of Technol., Yokohama, Japan)
SO Extended Abstracts of the 15th Conference on Solid State Devices and Materials, 1983, p. 11-14 of x+381 pp., 7 refs.
ISBN: 4 930813 04 2
Published by: Japan Soc. Appl. Phys, Tokyo, Japan
Conference: Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, Japan, 30 Aug.-1 Sept. 1983
Sponsor(s): Japan Soc. Appl. Phys
DT Conference; Conference Article
TC Practical; Experimental
CY Japan
LA English
AB Formation of CoSi2 by solid phase epitaxy is investigated. When the film is formed by the conventional SPE method, the film is not usually uniform and the surface of the sample is consisted of both Si area and formed CoSi2 area. The **two step annealing** method proposed is effective to improve the uniformity of the film, e.g. the Si area is drastically decreased. Patterning of the Si wafer before **silicide** growth is also effective to improve the uniformity. The growth kinetics of the **silicide** is also discussed

CC A6855 Thin film growth, structure, and epitaxy; B0510D Epitaxial growth; B2550 Semiconductor device technology; B2570 Semiconductor integrated circuits

CT annealing; cobalt compounds; epitaxial growth; integrated circuit technology; semiconductor technology

ST two step annealing; IC technology; CoSi2 films; patterning effects; solid phase epitaxy; Si area; Si wafer; silicide growth; growth kinetics

ET Si2; Co*Si; Co sy 2; sy 2; Si sy 2; CoSi2; Co cp; cp; Si cp; Si

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(FILE 'HOME' ENTERED AT 21:28:45 ON 17 OCT 2006)

FILE 'INSPEC' ENTERED AT 21:28:53 ON 17 OCT 2006

L1 16827 "TWO-STEP"
L2 148806 ANNEAL OR ANNEALING
L3 682 L1(5A) L2
L4 646 SALICIDE
L5 10 L3 AND L4
L6 9276 SILICIDE
L7 64 L3 AND L6
L8 59 L7 NOT L5